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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHAU, COREY P	
ART UNIT	**PAPER NUMBER**
2615	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/09/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/915,348	KODAMA, TOMOYA	
	Examiner	Art Unit	
	Corey P. Chau	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,8-10,14,24,30 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-10,14,24,30 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 1, recites "the control processor **makes reservation of sending an instruction**", which is written in a manner which is unclear to the examiner how to "**makes reservation of sending an instruction**" and what does mean to "**makes reservation of sending an instruction**".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 8-10, 14, 24, 30, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6275239 to Ezer.

6. Regarding Claim 1, as best understood with regards to the 112, 2nd problem mention above, Ezer discloses an audio processor which processes an input data stream via an external memory (103)(Fig. 1), comprising:

a control processor (101) to fetch in, when executing one of divided procedures of an audio process, a program and audio data corresponding to a next one of the procedures from the external memory (103) which stores programs and a group of data used for sequentially executing the divided procedures of the audio process (Figs. 5 and 6);

an internal memory (Fig. 4; claim 6) to store the program and audio data fetched from the external memory by the control processor and corresponding to the one and the next one of the procedures, the internal memory including an instruction memory configured to store an instruction group of the program transferred from the external memory and a data memory configured to store a data group transferred from the external memory (Figs. 2 and 7; column 3, lines 27-56; column 10, lines 16-40);

a coprocessor (102) to subserve the control processor to subject audio data of the input data stream to the divided procedures of the audio process sequentially (abstract; Figs. 8 and 9), based on the program fetched by the control processor (Figs. 1 and 2; column 1, line 60 to column 2, line 31).

Ezer does not expressly disclose the coprocessor executing multiplication/accumulation addition according to VLIW (Very Long Instruction Word). However, Examiner takes Official Notice that it would have been obvious to one having ordinary skill in the art to have the coprocessor execute multiplication/accumulation, addition according to VLIW (Very Long Instruction Word), wherein one VLIW instruction encodes multiple operations and therefore multiple operations can be handled at the same time, resulting in faster processing. Therefore it would have been obvious to one

having ordinary skill in the art at the time the invention was made to modify Ezer to have the coprocessor execute multiplication/accumulation, addition according to VLIW (Very Long Instruction Word), wherein one VLIW instruction encodes multiple operations and therefore multiple operations can be handled at the same time, resulting in faster processing.

Ezer as modified discloses:

a DMA controller to control writing of data to the external memory, writing of the instruction group to the instruction memory, and writing of the data group to the data memory, and reading of the data and the data group from the external memory and the data memory by DMA (Direct Memory Access) transfer (Figs. 2 and 7; column 3, lines 27-56; column 10, lines 16-40),

wherein the coprocessor subserves the control processor to perform the process based on the instruction group using reconstruction to generate audio data (Figs. 6-7; column 9, line 44 to column 10, line 40), and

wherein the control processor makes reservation of sending an instruction to the DMA controller so that the data and instruction group required for the next processing is prepared in advance while continuing the processing which is currently performed (Figs. 2 and 6-7; column 3, lines 27-56; column 9, line 44 to column 10, line 40)

7. Regarding Claim 2, Ezer as modified discloses the coprocessor is configured to subserve the control processor to subject sequentially the audio data to decoding, noise-less decoding, noise reduction, filter bank, and block switching in accordance with

the programs and data fetched from the external memory in units of one procedure (Figs. 8 and 9; column 10, line 41 to column 11, line 42).

8. Regarding Claim 3, Ezer as modified discloses the coprocessor (102) is configured to subserve the control processor to execute the program fetched in the internal memory from the external memory in accordance with progress of the procedures of the audio process (Fig. 4).

9. Regarding Claim 8, Ezer as modified discloses the control processor sequentially transfers a plurality of program modules corresponding to procedures of the audio process to the coprocessor from the external memory according to the progress of the procedures (Figs. 1 and 2; column 1, line 60 to column 2, line 31).

10. Regarding Claim 9, Ezer as modified discloses the coprocessor (102) subserves the control processor to execute decoding of bit stream data, noiseless decoding, inverse quantization, scale factor, TNS processing, filter bank processing, and the block switching, in this order, to reconstruct audio data (Figs. 8 and 9; column 10, line 41 to column 11, line 42).

11. Regarding Claim 10, Ezer as modified discloses the control processor includes a function of predicting which procedure is performed after the procedure which is currently performed (Figs. 4 and 6).

12. Regarding Claim 14, Ezer as modified discloses the control processor is further configured to release a storage region of the internal memory occupied by the data stored in the internal memory or a program if the data stored in the internal memory or the program becomes unused by the coprocessor (Figs. 2, 4, 7, and 9).

13. Regarding Claim 24, Ezer as modified discloses the internal memory includes an instruction memory and a data memory, and at least two parallel busses lead from the instruction memory and the data memory to the coprocessor (Fig. 4).

14. Regarding Claim 30, Ezer as modified discloses an audio input/output interface (Fig. 1); and an internal bus; wherein the internal bus links the control processor, the coprocessor and the audio input/output interface together (Figs. 4).

15. Regarding Claim 34, Ezer as modified discloses the divided procedures of the audio process include five different processing stages performed sequentially, the five different processing stages using different memory spaces of the data memory in the internal memory (Figs. 8 and 9; column 10, line 41 to column 11, line 42).

Response to Arguments

16. Applicant's arguments filed 12/22/2006 have been fully considered but they are not persuasive.

17. With respect to Applicant's argument on page 7, stating that "Ezer fails to teach reservation of sending an instruction to the DMA controller so that the data and instruction group required for the next processing is prepared in advance while continuing the processing which is currently performed", has been noted. However, the examiner respectfully disagrees. Ezer does disclose "reservation of sending an instruction to the DMA controller so that the data and instruction group required for the next processing is prepared in advance while continuing the processing which is currently performed" as shown in Figs. 2, and 6-7; column 9, line 44 to column 10, line

40, "example of time-division multiplexing is illustrated in FIG. 6. Within an update period (e.g., 1/30 or 1/60 second), the CPU performs application, system, input, control, and update functions 602. The MBP decodes audio and video VLC's 603 and 604. The MSP performs audio decode and filtering 605; video iQ and iDCT 606; and 3-D graphics transform, lighting, and setup 607. The MDP performs clear, copy, and composite images 608; video motion compensation and reconstruction 609; and 3-D graphics primitive drawing 610. More specifically, at the vertical interval, **the CPU software switches display buffers and performs an audio direct memory access (DMA) output to the next set of audio buffers**. Afterwards, the CPU commands the MDP to begin initializing the next display buffer by clearing the color and depth images, copying background images, or compositing video images. **Meanwhile, the MBP decodes audio digital bitstream packets and passes the packets to the MSP to perform audio decompression and filtering on the data. When the audio and display processing for the next update is complete, the CPU directs the MBP to decode video digital bitstream packets and passes them to the MSP for inverse quantization and discrete cosine transforms, while the MDP performs motion compensation and reconstruction with the MSP output. When video processing for the next update is complete, the CPU commands the MSP to transform and setup the 3-D graphics data for the next update. Thereupon the MSP commands the MDP to draw the 3-D graphics primitives it had processed. Meanwhile, the CPU reads input devices and script information and prepares of the next update and then waits for the next vertical interval.** It should be noted that the update period

should be balanced with the amount of processing to be performed within it in order to sustain a particular update rate. If the processing has not yet completed by the appropriate next vertical interval, the CPU software decides whether to delay the buffer switch and complete the update processing or to terminate processing, switch buffers, and proceed to process the next update. Audio processing must continue to generate audio buffers at the output sample rate.

FIG. 7 shows a data structure for performing the partitioning scheme of the present invention. Because the MSP is a physical address, single context processor with on-chip data and instruction RAMs, software is designed to efficiently use MSP resources for the several functions which are performed in each update period. A small amount of resident dispatcher code 701 in the MSP Instruction Memory (Imem) 702 **reads code for the next function to be performed from a task list 703 updated by the CPU.** The task list contains code and data addresses and lengths. The MSP then initiates a DMA transfer of the task code into Imem 702 and then jumps to the starting address within the task (e.g., 3-D graphics task 704, audio task 705, video task 706, etc.). The task initiates DMA transfers of input data buffers from DRAM 707 to Data Memory (Dmem) 708, where it process the data and generates output buffers for DMA back into DRAM 707. MSP Dmem 808 contains a resident data portion 709, input buffer 710, working buffer 711, and output buffer 712. The MDP command interface may DMA directly from MSP Dmem or from DRAM. When complete, the task returns to the dispatcher code. Tasks are constructed to fit entirely into Imem in order to minimize code swapping.

Tasks organize data access so that the DMA of the input and output buffers in Dmem occur in parallel with processing data in the MSP".

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey P. Chau whose telephone number is 571-272-7514. The examiner can normally be reached on Monday-Friday, 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 2, 2007
CPC

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